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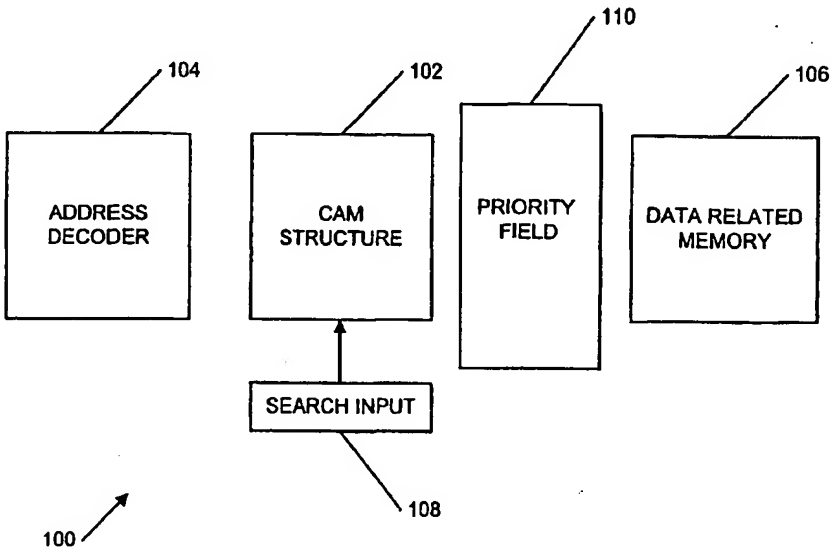
(54) Title: MATCH RESOLUTION CIRCUIT FOR AN ASSOCIATIVE MEMORY




(57) Abstract: A system and method for determining a best match from a plurality of matches received in response to a search input for an associative memory includes a priority field associated with each data item stored in the associative memory. The priority field corresponds to criteria that is used to order the priority of the data items in the associative memory. A match resolution circuit is coupled to receive match signals from an associative memory, such as a CAM, and the priority fields of the matching data items. The match resolution structure compares the priority fields of the matching data items to determine which data item has the highest priority. The match resolution structure indicates the data item with the highest priority in the priority field as the best match of the associative memory for the particular search input.

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# MATCH RESOLUTION CIRCUIT FOR AN ASSOCIATIVE MEMORY

## RELATED APPLICATION

The subject matter of the present application is related to and claims priority, under 35 U.S.C. § 119(e), from U.S. provisional patent application serial no. 60/148,403, entitled "Match Resolution Circuit for Content Addressable Memory " by Alex E. Henderson and Walter E. Croft, which application was filed on August 11, 1999 and is incorporated herein by reference.

## BACKGROUND

### A. Technical Field

The present invention relates generally to associative memories, and in particular to content addressable memories. More particularly, the present invention relates to an associative memory having a match resolution circuit for determining a best match from among multiple matches.

### B. Background of the Invention

An associative memory, such as a content addressable memory (CAM), is a device that permits the contents of the memory to be searched and matched instead of having to specify a memory location address in order to retrieve data from the memory. A CAM may be used to accelerate any application requiring fast searching of a database, list, or pattern, such as in database machines, image or voice recognition, or computer and communication networks. A CAM provides a performance advantage over conventional memory devices with conventional memory search algorithms, such as binary or tree-based searches, by comparing the desired information against the entire list of entries simultaneously, giving an order-of-magnitude reduction in search time. For example, a binary search through a database of 1000 entries may take ten separate search steps whereas a CAM device with 1000 entries may be searched in a single operation resulting in a search which takes ten times less time. One example of an application in which CAM devices are often used is to store a routing table for high speed switching systems which need to rapidly search the routing table to look for a matching destination address so that a data packet may be routed to the appropriate destination address.

A CAM device is organized somewhat differently from typical SRAM or DRAM devices. Information stored in a CAM may be accessed by comparing the data stored in the memory with data placed in a special register known as a search input or compare register as

opposed to RAM devices in which information is accessed by specifying a particular memory address. If there is a match in particular memory locations with every corresponding bit in the register, a Match Flag is asserted to let the user know that the data in the register was found in the CAM device. Thus, with a CAM device, the user supplies a piece of data she would like to match to the CAM and gets back the address of any matching pieces of data in the CAM. There are two common types of CAM memory, binary CAM and ternary CAM. Binary cam requires an exact match of all bits in the search input and comparand for a match. Ternary CAM uses a mask to allow some bits to be treated as "don't care" bits and ignored in the determination of a match.

Data in a Binary CAM location typically comprises 2 fields: a comparand and an associated data field. Unlike a random access memory ("RAM"), when a search is performed on a CAM, all comparands in a CAM are compared simultaneously with a search input stored in a register. As each comparand is compared with the search input, a match line for that comparand is activated if the comparand matches the search word. Prior art ternary CAM devices may also contain an additional field known as a mask. The mask may be used to filter off portions of the comparand during the search procedure. In other words, the mask allows a comparison between the search input and only certain portions of the comparand as determined by the mask.

A search on a CAM may result in several matches in response to the search input, however, only one result should be returned. Therefore, one problem in the prior art is determining which match from a plurality of matches should be returned as the best match for a particular search input. One solution in the prior art is to implement a priority resolution circuit that uses the position of the data item in the CAM array to determine which match to output. One disadvantage in using a priority resolution circuit based on the position of the data item in the CAM array is that it only offers one criteria, (i.e. position) for determining a best match. Additionally, in order to change the priority of a particular CAM data item, it is necessary to move the data items to different positions in the CAM array. This process is cumbersome and slows down the operation of the CAM.Accordingly it is desirable to provide a priority resolution system that is capable of determining a best match among a plurality of CAM matches.. More specifically, it is advantageous to provide a priority resolution system that can be dynamically updated and can use criteria other than position to determine a best match among a plurality of matches.

## SUMMARY OF THE INVENTION

The present invention overcomes the deficiencies and limitations of the prior art with a unique system and method for determining a best match from a plurality of matches resulting in response to a search input performed on an associative memory. The system and method for determining a best match from a plurality of matches comprises a priority field associated with each data item stored in the associative memory. The priority field corresponds to criteria that is used to order the priority of the data items. A match resolution module is coupled to receive match signals from an associative memory and the priority fields associated with the matching data entries. The match resolution structure compares the priority fields of the plurality of matching data items to determine which data item has the highest priority. The match resolution structure then indicates the data item having the highest priority as the best match of the associative memory for the particular search input.

These and other features and advantages of the present invention may be better understood by considering the following detailed description of preferred embodiments of the invention. In the course of this description, reference will be frequently made to the attached drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of one embodiment of a CAM including a priority field in accordance with the present invention.

Fig. 2 is a block diagram of one embodiment of a CAM including a match resolution circuit.

Fig. 3 is a block diagram of one embodiment of a method for determining a best match.

Fig. 4 is a block diagram illustrating one embodiment of a match resolution circuit for a CAM.

Fig. 5 is a block diagram of another embodiment of a match resolution circuit for a CAM.

Figs. 6a-6d are block diagrams of other embodiments of a match resolution circuit for a CAM.

Fig. 7 is one embodiment of a hierarchical match resolution circuit for a CAM.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention is particularly applicable to a content addressable memory (CAM) device, such as that used as a single or dual port CAM memory, an event-co-processor, and a database co-processor, and it is in this context that the invention will be described. It will be appreciated, however, that the match resolution module in accordance with the invention has greater utility and may be used with any type of associative memory that accesses data based upon the content of the stored data (rather than the location in which that data is stored) and provides multiple matches in response to a search input.

Referring now to Figure 1, there is shown one embodiment of a CAM having a match resolution circuit in accordance with the present invention. The CAM structure comprises a CAM match structure 102 for storing CAM words or data items, an address decoder 104 for addressing the CAM when initially storing data items, and a related memory 106 which may be a random access memory (RAM) or a read-only memory (ROM). Typical CAM usage involves locating a data item in the CAM match structure 102. A data item is specified by entering a search input 108 which compares simultaneously all of the data items stored in the CAM match structure 102 with the search input 108. A typical CAM search may result in finding a plurality of data items which match the search input 108. In order to determine a "best match" for the particular search input 108, a priority field 110 associated with each data item is evaluated to determine a best match from the plurality of matches. A best match can be determined by an arithmetic or logical comparison of the priority fields 110 of all matching CAM data items. When a best match is found for a particular search input 108, the apparatus can retrieve additional information concerning the requested data item from the related memory 106. As used herein, a "best match" is used to define a single data item from a plurality of data items that match the search input 108. As one skilled in the art will readily understand, a best match does not imply that there is only one true absolute match but that in the context of the priority field 110, there is one data item which will be considered to be a best match and will be outputted by the CAM. Examples of various best matches, priority fields, and criteria are discussed in more detail below.

As discussed above, the present invention provides a priority field 110 associated with each word of the CAM. The priority field 110 allows each data item to be prioritized according to some criteria. In a preferred embodiment, a priority field 110 comprises 16 bits. One skilled in the art will realize that the number of bits comprising the priority field 110 will depend on the number of bits required to uniquely identify the priority associated with a data item. The priority field 110 may correspond to any number of criteria, including but not

limited to, a weight field stored in the CAM match structure 102, length of the longest contiguous unmasked field in the CAM match structure 102, the total number of unmasked bits in the CAM match structure 102, the total number of matching bits resulting from a compare, the path length metric derived from a routing protocol such as OSPF, the order of an order dependent list such as an Access Control List for a router, or position in the CAM match structure. Thus, the present invention advantageously allows the use of a variety of criteria for ordering the priority of each data item.

Additionally, because the priority field is a separate field for indicating the priority of the data item, the priority of the various data items may be changed by changing the entry in the priority field. For example, assume a CAM structure contains a first data item A, a second data item B, and a third data item C. Further assume that the first data item A has a priority field indicating that it has a priority of 1, the second data item B has a priority field indicating that it has a priority of 2, and the third data item C has a priority field indicating that it has a priority of 3. If priority is determined according to the priority field with the highest number, then the third data item C, which has a priority of 3, has the highest priority. However, if for some reason it is necessary to change the priority of the data items, the priority of a data item may be changed simply by changing the priority field. For example, assume that the priority field for the first data item A is changed from 1 to 3 and the priority field for the third data item C is changed from 3 to 1, then using the same convention that priority is determined according to the highest number, the first data item A, which now has a new priority of 3, has the highest priority. Thus, the present invention advantageously provides a simple mechanism for changing the priority of data items by changing the priority in the priority field.

The present invention also provides for hierarchical match resolution. In other words, if two or more CAM data items have the same priority according to one priority field criteria, then a second priority field criteria can be applied to these entries to determine a best match. A preferred embodiment for a hierarchical match resolution system for a CAM is described below in more detail with reference to Figure 6.

Referring now to Figure 2 and Figure 3, there are shown a functional block diagram of one embodiment of a CAM including a match resolution circuit and a block diagram of one embodiment of a method for determining a best match from a plurality of matches. The CAM structure 200 comprises a CAM structure 102 coupled to receive a search input 108. The CAM structure 102 receives (302) the search input 108 and compares (304) the search

input 108 to all the data item entries in the CAM structure 102 as described above. The CAM structure 102 then generates (306) a match signal (not shown) for all CAM data items in the CAM that match the search input 108. The CAM structure 102 then outputs the match signal and the priority field (not shown) to the match resolution circuit 202. The match resolution circuit 202 evaluates (308) the priority field for each matching CAM data item and determines (310) which priority field has the highest priority. The output of the match resolution circuit 202 then indicates (312) the CAM data item with the highest priority according to the priority field. The indicated item is considered the best match for the particular search input 108. Preferably, the output of the match resolution circuit 204 comprises either prioritized match signals or the address of the highest priority matching entry.

Referring now to Figure 4, there is shown a block diagram illustrating one embodiment of a CAM match resolution circuit. A CAM match resolution circuit in accordance with the present invention comprises a first two port priority resolution circuit 402, a second two port priority resolution circuit 404, and a third two port priority resolution circuit 406. The first and second two port priority resolution circuits, 402 and 404, are each coupled to receive a match signal and a priority field associated with two CAM data items. For example, the first two port priority resolution circuit 402 is coupled to receive a first match signal 408a and a first priority field signal 408b from one CAM data item, and a second match signal 410a and a second priority field signal 408b from a second CAM data time. The first two port priority resolution circuit 402 determines which CAM data item has the higher priority according to the inputted match and priority field signals and outputs the match signal 416a and the priority field signal 416b with the highest priority. Similarly, the second two port priority resolution circuit 404 is coupled to receive a first match signal 412a and a first priority field signal 412b from one CAM data item, and a second match signal 414a and a second priority field signal 414b from a second CAM data item. The second two port priority resolution circuit 404 determines which CAM data item has the higher priority according to the inputted match and priority field signals and outputs the match signal 418a and the priority field signal 418b with the highest priority. The third two port priority resolution circuit 406 then compares the results from two port priority resolution circuit 402 and two port priority resolution circuit 404 and outputs the match signal 420a and the priority field signal 420b with the highest priority. For example, if the priority field signal corresponds to an assigned priority number, then the CAM data item with the highest priority

number would be outputted from two port priority resolution circuit 406. One skilled in the art will recognize that the present invention is not limited to only determining the "highest priority" but that the principles of the present invention can also be used to determine and output the data item with the "lowest" priority. Thus, a CAM match resolution circuit can be implemented as a stack of two entry match resolution circuits wherein each two entry match resolution circuit compares two input values and outputs the greater value. The present invention is not limited to the use of three two port priority resolution circuit in a two stage circuit for determining a best match, but one skilled in the art will realize that the principles of the present invention may be applied to any number of two port priority resolution circuit arranged in the necessary number of stages for comparing the priority fields of any number of data items..

Referring now to Figure 5, there is shown a block diagram of one embodiment of one row of a match resolution circuit for a CAM. The match resolution circuit 500 comprises a priority field Most Significant Bit (MSB) component 502, a compare MSB and OR plane output component 504, a match signal 508, an AND gate 506, and a MSB OR plane 512. As indicated in Figure 5, the match resolution circuit of the present invention incorporates each of these elements for each bit in the priority field. In other words, the bits in the priority field for a data item are evaluated serially. Figure 5 illustrates these elements for only two bits of the priority field in the interest of simplicity. In a preferred embodiment, the match signal 508 is the high order bit of the priority field. For the first bit in the priority field, the match signal 508a and the priority field MSB are ANDed together and outputted to the MSB OR plane 512a. The result of the MSB OR plane 512a is compared with the MSB of the priority field received from the priority field MSB 502a. The result is then used as compare ok or enable signal for the next AND gate 506b for the next comparison. This process is repeated until a determination of the best match is made. Thus, the most significant bit of all priority fields are compared to the result of the OR plane. If the priority field bit matches the result a compare OK signal is propagated to the next less significant bit. The OR function can also be implemented using pre-charge logic as shown in figure 6b.

Referring now to Figure 6a, there is shown another embodiment of a match resolution circuit for a CAM in accordance with the present invention. The embodiment described in detail in Figure 5 can be implemented using a "look ahead" logic similar to an adder circuit. The addition of a "look ahead" logic advantageously improves the speed of the match resolution circuit. In another embodiment, the MSB OR plane 512 can be implemented using

wide gate structures as described in U.S. Patent No. 5,999,435, entitled "Content Addressable Memory Device," by Alex E. Henderson and Walter E. Croft, which patent is incorporated herein by reference in its entirety.

Figure 6b is a precharge logic implementation of the circuit of figure 6a. The OR function is implemented by pre-charge transistor 600b, pulldown transistor 601b (one per cell) and inverter 602b. Transfer gate 603b and transistor 604b implement the AND function. The compare function is implemented by the pre-charge logic complex gate comprising transistors 605b through 609b and inverter 610b. Transistors 605b and 609b are controlled by a timing signal generated by a dummy row or other timing method. The timing strobe is required to prevent a false enable out from corrupting the result of the next cell. The timing circuits are designed so that the timing strobe occurs after the OR feedback line is stable.

Figure 6c is a faster version of the circuit of figure 6b. The pre-charge logic OR has been divided into multiple sub-circuits comprising N rows (transistors 600c, 601c and inverter 602c). The results of the sub-circuits are combined by a second OR circuit comprising transistors 603c and 604c. This reduces the loading on the first layer OR resulting in increased speed and combines the feedback and second level OR function.

Figure 6d is a diagram of a match resolution circuit that implements a multi-bit priority resolution to further increase speed. Multiple priority bits are decoded and used to drive multiple OR planes. The results of the OR functions are encoded to generate an enable output. The pre-charge implementations of the OR functions described in 6b and 6c can be used to implement the OR planes. For a two bit priority resolution circuit the decodes x1, 1x and 11 can be used as inputs to the OR planes.

Referring now to Figure 7, there is shown one embodiment of hierarchical match resolution circuit for a CAM. The hierarchical match resolution circuit for CAM cascades two or more match resolution circuits, 702 and 704, such that if there are multiple "best" matches based on a first criteria (e.g. network path length), a second criteria (e.g. link speed) can be used to determine the best match. A hierarchical match resolution circuit for a CAM comprises a CAM structure 102 coupled to receive an input search 108, a first match resolution module 702, and a second match resolution module 704. As described above, the CAM structure 102 receives a search input 108 and compares the search input 108 to all the CAM data items. The CAM structure 102 then generates a match signal for each data item which matches the search input 108. The search result of the CAM may result in a plurality of data items which match the search input 108. In such instances, a first match resolution

circuit 702 is coupled to receive the match signals and the first priority fields associated with each CAM data item that matched the search input 108. The first match resolution circuit 702 evaluates the first priority field of each of the matching items and determines which data item has the highest priority based on the first priority fields. The first match resolution circuit 702 may result in multiple data items having equal priority based on the first priority field (e.g. when network path length is used). The second priority fields are then evaluated to determine a best match best on the second priority field with the highest priority. The data item with the second priority field with the highest priority is then outputted as the best match. One skilled in the art will recognize that the present invention is not limited to two match resolution circuits but that any number of match resolution circuits may be implemented to determine a best match using several criteria. Additionally, for each additional criteria used for determining priority, an additional priority field is associated with each data item. Thus, if two criteria are used for determining priority in a hierarchical match resolution circuit, then preferably each data item includes a first priority field and a second priority field. Similarly, if three criteria are used for determining priority in a hierarchical match resolution circuit, then preferably each data item includes a first priority field, a second priority field, and a third priority field. Thus, the present invention advantageously allows more than one criteria to be used to determine a best match from a plurality of matches resulting from a CAM search.

From the above description, it will be apparent that the invention disclosed herein provides a novel and advantageous system and method for determining a best match from a plurality of matches determined in response to a search item. The foregoing discussion discloses and describes merely exemplary methods and embodiments of the present invention. As will be understood by those familiar with the art, the invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. Accordingly, the disclosure of the present invention is intended to be illustrative, but not limiting, of the scope of the invention, which is set forth in the following claims.

We claim:

1. A match resolution structure for selecting a best match from a plurality of matches, the plurality of matches determined in response to a search input for an associative memory, the structure comprising:

a plurality of match inputs, each match input receiving a priority field for indicating a priority of the match input; and

a match resolution logic, coupled to receive the priority field from at least two match inputs, for comparing the priority fields and indicating a best match..

2. The structure of claim 1 wherein the priority field contains the length of the longest contiguous unmasked field in the data item.

3. The structure of claim 1 wherein the priority field contains the total number of unmasked bits in the data entry.

4. The structure of claim 1 wherein the priority field contains the prefix length of an IP address.

5. The structure of claim 1 wherein the priority field contains a path length metric derived from a routing protocol such as OSPF.

6. The structure of claim 1 wherein the priority field contains the order of an order dependent list such as an Access Control List for a router.

7. The structure of claim 1 wherein the priority field for a data item may be changed to indicate a change in priority for that data item.

8. The structure of claim 1 wherein the match resolution logic comprises a stack of two port priority resolution circuits.

9. The structure of claim 1 further comprising a second priority field associated with each data item.

10. The structure of claim 1 wherein the associative memory is a CAM.

11. A method of operation for a match resolution circuit, the match resolution circuit being coupled to receive a plurality of data items from an associative memory, each data item having an associated priority field, the method comprising:

receiving a plurality of match signals for the plurality of data items; and

comparing the priority field and the match signals for the data items to determine a best match.

12. The method of claim 11 wherein the priority field contains the length of the longest contiguous unmasked field in the data item.

13. The method of claim 11 wherein the priority field contains the total number of unmasked bits in the data entry.

14. The method of claim 11 wherein the priority field contains the position of data item.

15. The method of claim 11 wherein the data item further includes a second priority field, the method further comprising the step of:

comparing the second priority field associated with the data items for determining a best match.

16. The method of claim 11 wherein the associative memory is a CAM.

17. An associative memory structure for storing and prioritizing a plurality of data items in the associative memory, the structure comprising:

a match structure for storing a plurality of data items, each data item having a priority field for prioritizing the plurality of data items; and

a search input, for receiving a search item that is compared simultaneously with the plurality of data items.

18. The structure of claim 17 wherein the first priority field contains the length of the longest contiguous unmasked field in the data item.

19. The structure of claim 17 wherein the associative memory is a CAM.

20. A method for selecting a best matching data item from a plurality of matching data items determined in response to a search input, each matching data item having a priority field, the method comprising:

receiving the priority field for each matching data item;

evaluating the priority field for each matching data item; and

selecting a best matching data item by selecting the priority field with the highest priority.

21. The method of claim 20 wherein each matching the priority field contains the length of the longest contiguous unmasked field in the data item.

22. The method of claim 20 wherein the priority field contains the total number of unmasked bits in the data entry.

23. The method of claim 20 further comprising the step of:

altering the priority of at least one data item by changing the priority field of at least one data item.

24. A match resolution circuit for selecting a best matching data item from at least a first data item and a second data item, the at least first data item and second data item matching a

search input for an associative memory, the first data item including a first priority field and the second data item including a first priority field, the circuit comprising:

a first input for receiving the first priority field of the first data item;

a second input for receiving the first priority field of the second data item; and

a compare circuit for comparing the first priority field of the first data item and the first priority field of the second data item and for indicating the first priority field with the highest priority.

25. The circuit of claim 24 wherein the first and second priority field contain the length of the longest contiguous unmasked field in the data item

26. The circuit of claim 24 wherein the first and second priority field contain the total number of unmasked bits in the data item.

27. The circuit of claim 24 wherein the associative memory is a CAM.

28. The circuit of claim 24 wherein the first data item and the second data item each further include a second priority field, the circuit further comprising:

a third input for receiving the second priority field of the first data item;

a fourth input for receiving the second priority field of the second data item; and

a second compare circuit for comparing the second priority field of the first data item and the second priority field of the second data item and for indicating the second priority field with the highest priority.

29. A match resolution circuit for indicating a best match from a plurality of matches received from an associative memory, the circuit comprising:

a plurality of inputs for receiving a priority field associated with the plurality of matches; and

a compare circuit, coupled to receive the plurality of inputs, for evaluating the priority fields associated with the plurality of matches, and indicating a best match from among the plurality of matches.

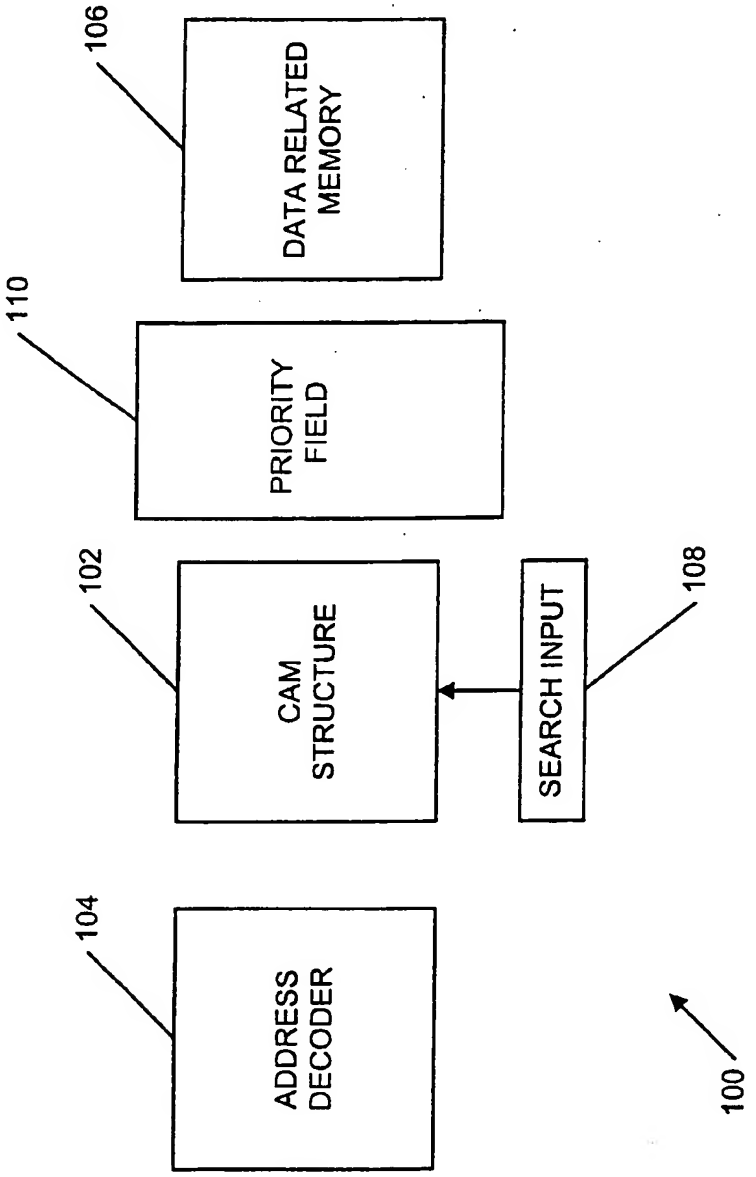
106
DATA RELATED MEMORY
110
PRIORITY FIELD
102
CAM STRUCTURE
SEARCH INPUT
108
104
ADDRESS DECODER
100

FIGURE 1

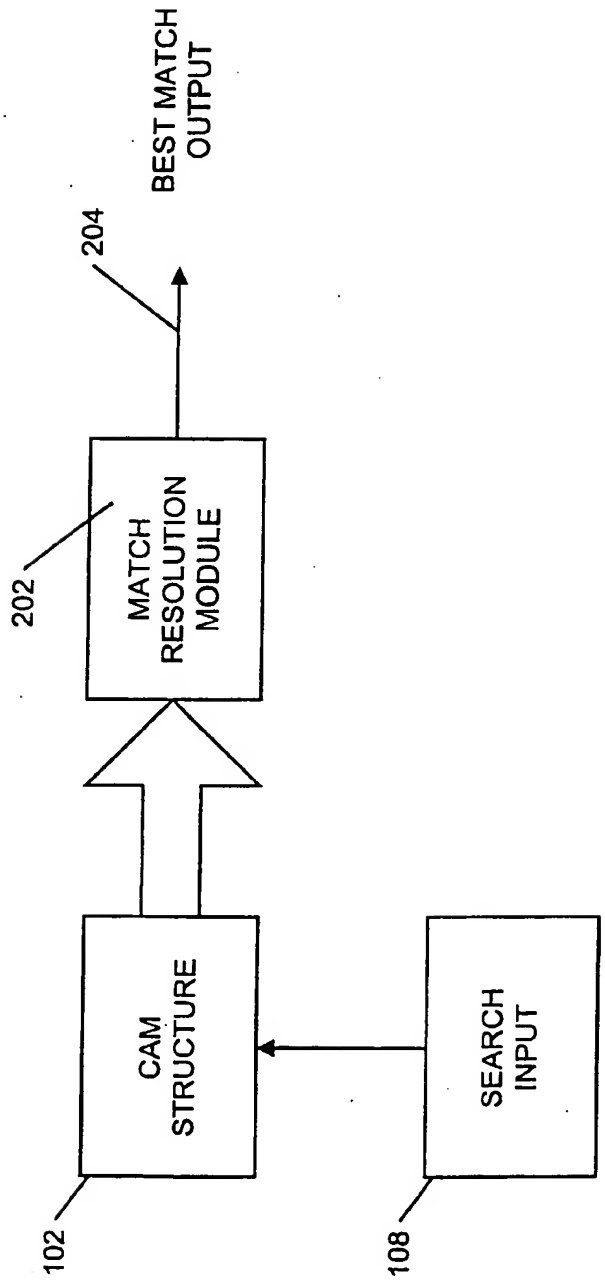
BEST MATCH OUTPUT
204
MATCH RESOLUTION MODULE
202
CAM STRUCTURE
102
SEARCH INPUT
108
200

FIGURE 2

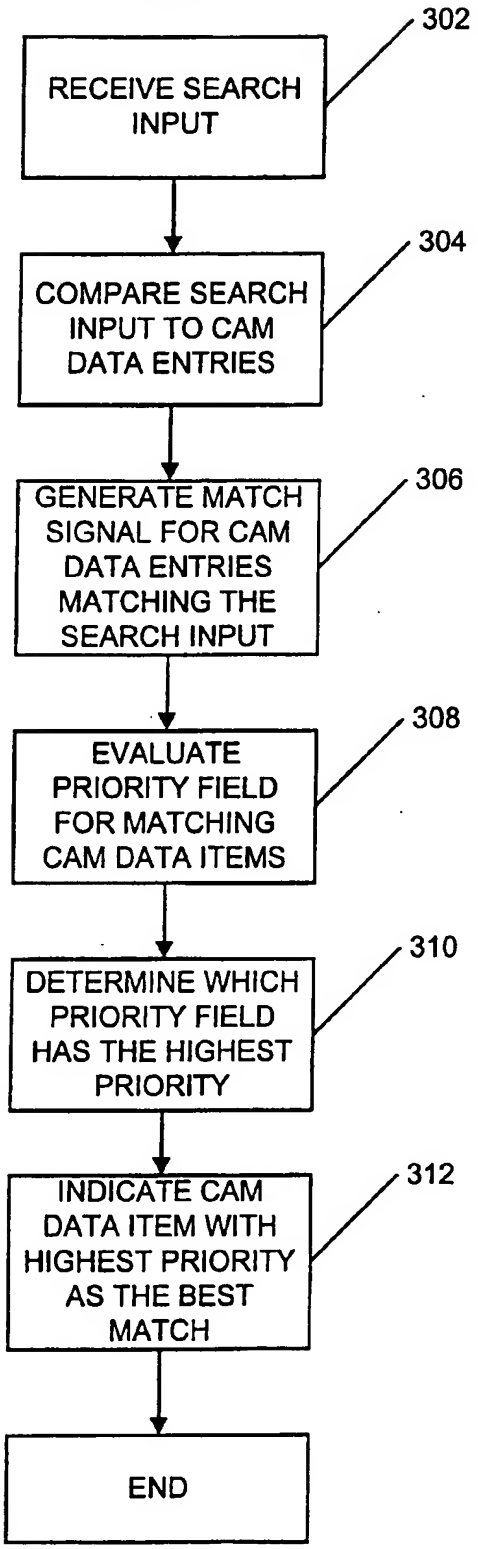
302
RECEIVE SEARCH INPUT
304
COMPARE SEARCH INPUT TO CAM DATA ENTRIES
306
GENERATE MATCH SIGNAL FOR CAM DATA ENTRIES MATCHING THE SEARCH INPUT
308
EVALUATE PRIORITY FIELD FOR MATCHING CAM DATA ITEMS
310
DETERMINE WHICH PRIORITY FIELD HAS THE HIGHEST PRIORITY
312
INDICATE CAM DATA ITEM WITH HIGHEST PRIORITY AS THE BEST MATCH
END

FIGURE 3

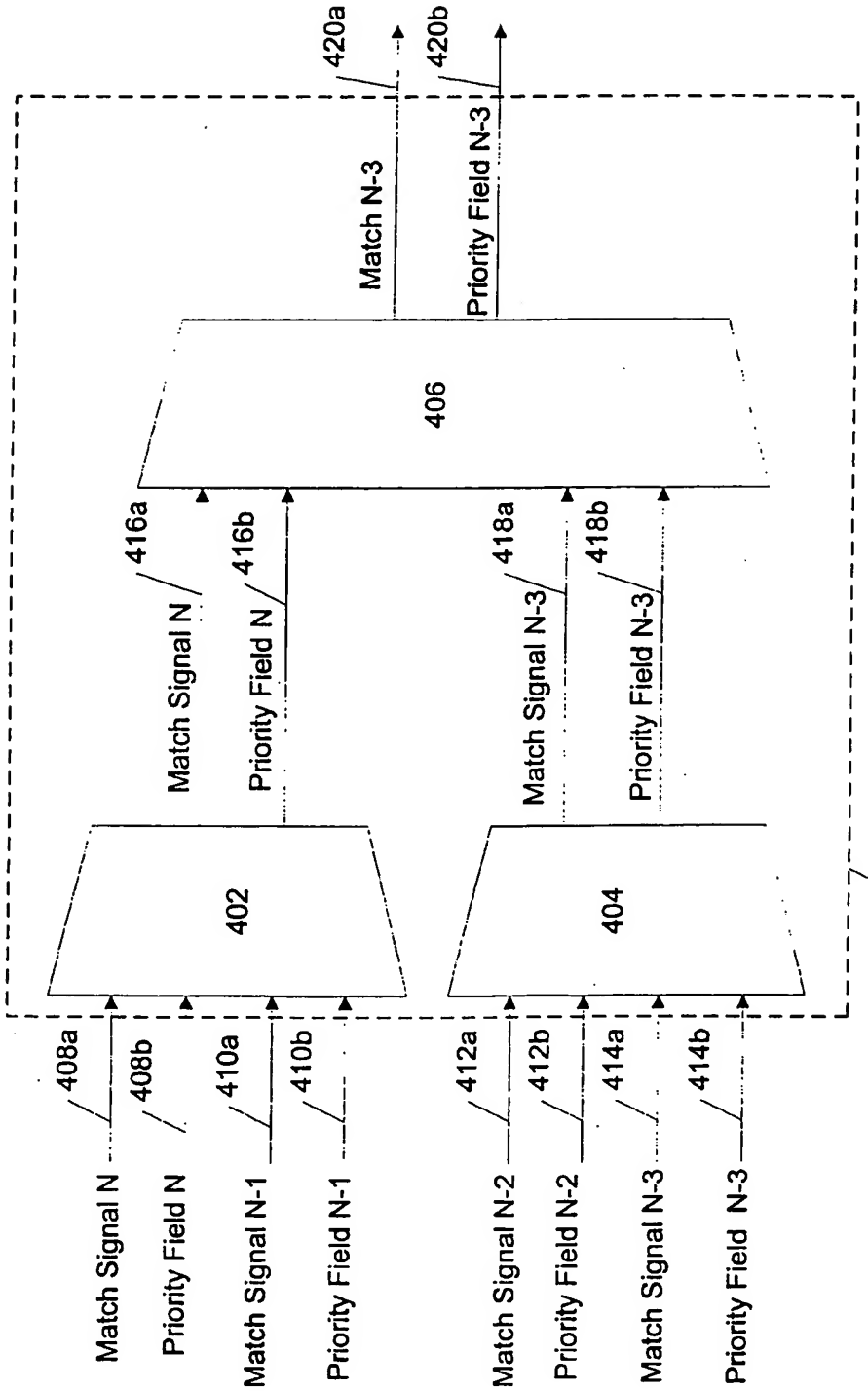
420a
420b
Match N-3
Priority Field N-3
406
416a
416b
418a
418b
Match Signal N
Priority Field N
Match Signal N-3
Priority Field N-3
402
404
202
408a
408b
410a
410b
412a
412b
414a
414b
Match Signal N
Priority Field N
Match Signal N-1
Priority Field N-1
Match Signal N-2
Priority Field N-2
Match Signal N-3
Priority Field N-3

FIGURE 4

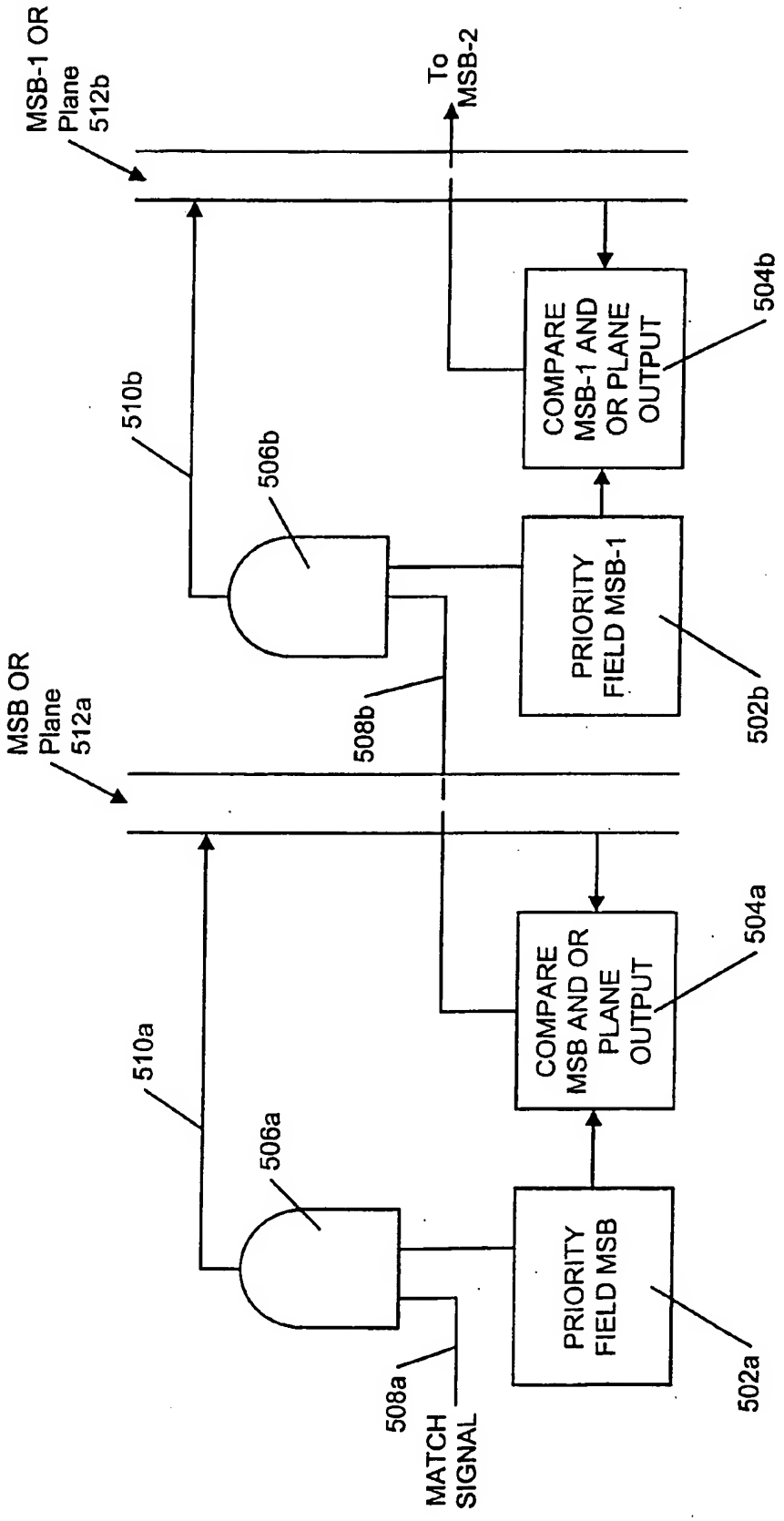
MSB-1 OR Plane 512b
To MSB-2
COMPARE MSB-1 AND OR PLANE OUTPUT
504b
510b
506b
PRIORITY FIELD MSB-1
502b
MSB OR Plane 512a
508b
COMPARE MSB AND OR PLANE OUTPUT
504a
510a
506a
PRIORITY FIELD MSB
502a
508a
MATCH SIGNAL
500

FIGURE 5

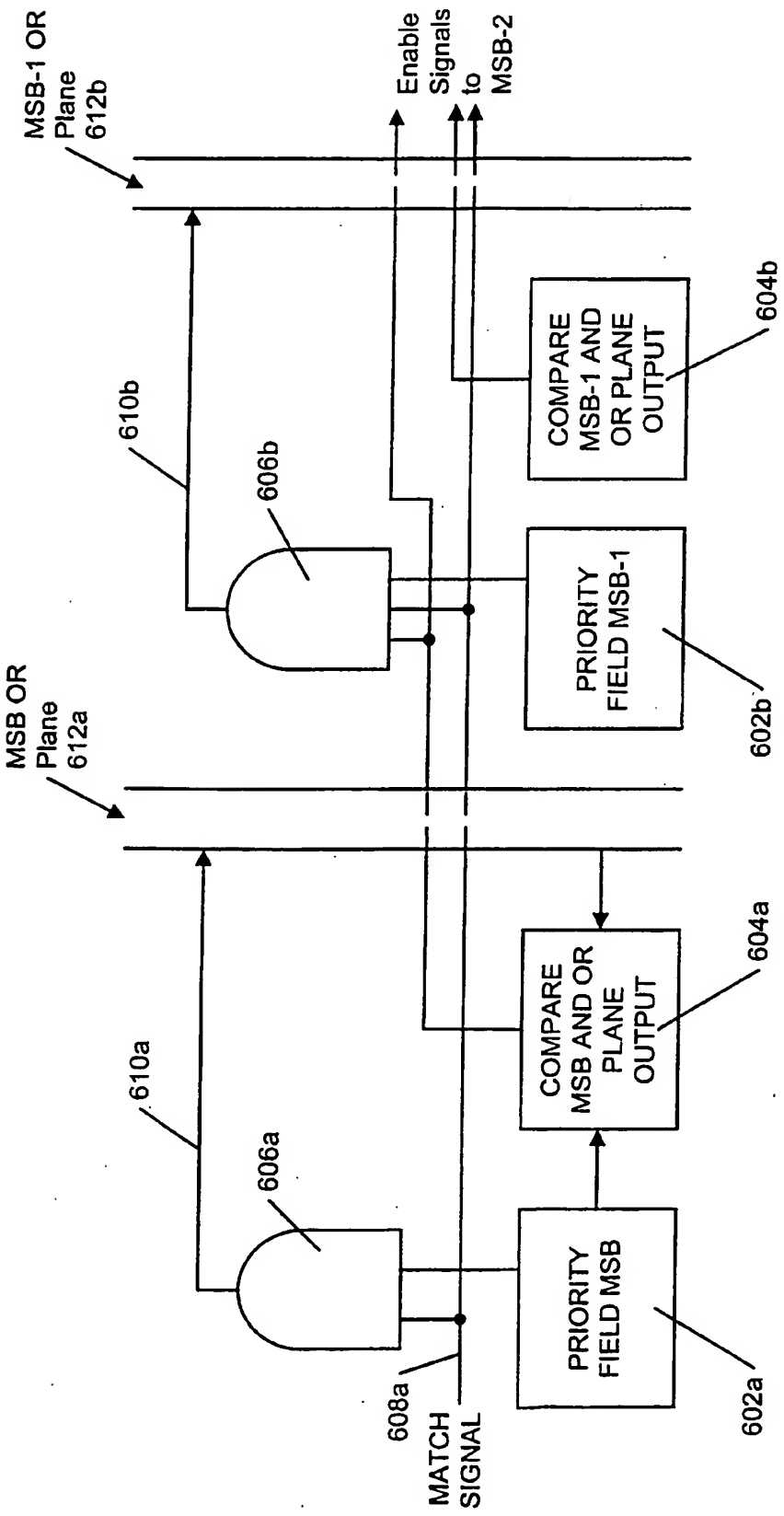
MSB-1 OR Plane 612b
Enable Signals to MSB-2
610b
606b
COMPARE MSB-1 AND OR PLANE OUTPUT
604b
PRIORITY FIELD MSB-1
602b
MSB OR Plane 612a
610a
606a
COMPARE MSB AND OR PLANE OUTPUT
604a
PRIORITY FIELD MSB
602a
608a
MATCH SIGNAL
600

FIGURE 6A

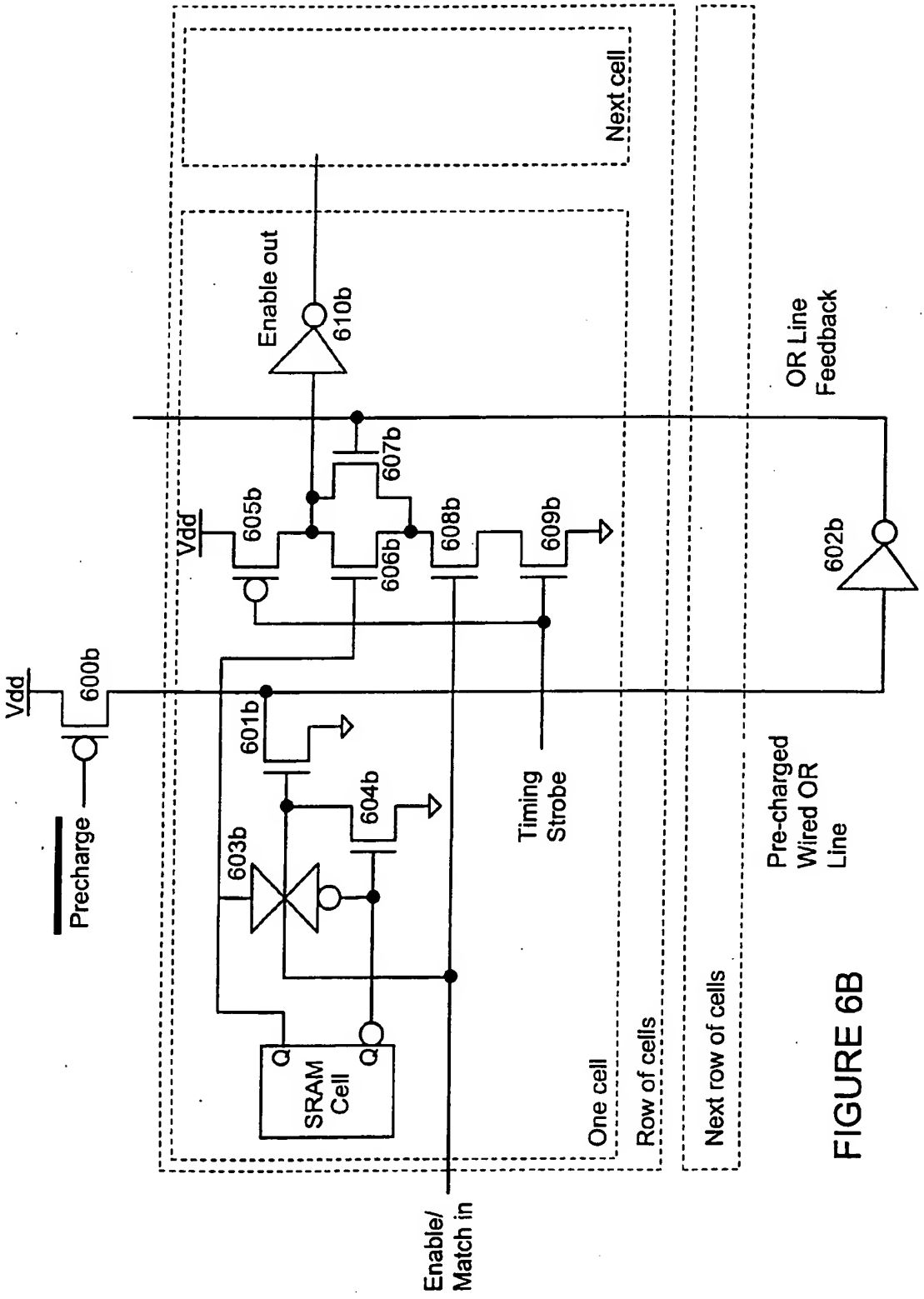
Next cell
Enable out
610b
OR Line Feedback
607b
Vdd
605b
606b
608b
609b
602b
Vdd
600b
601b
604b
603b
Timing Strobe
Precharge
Pre-charged Wired OR Line
SRAM Cell
Q
Q
One cell
Row of cells
Next row of cells
Enable/ Match in

FIGURE 6B

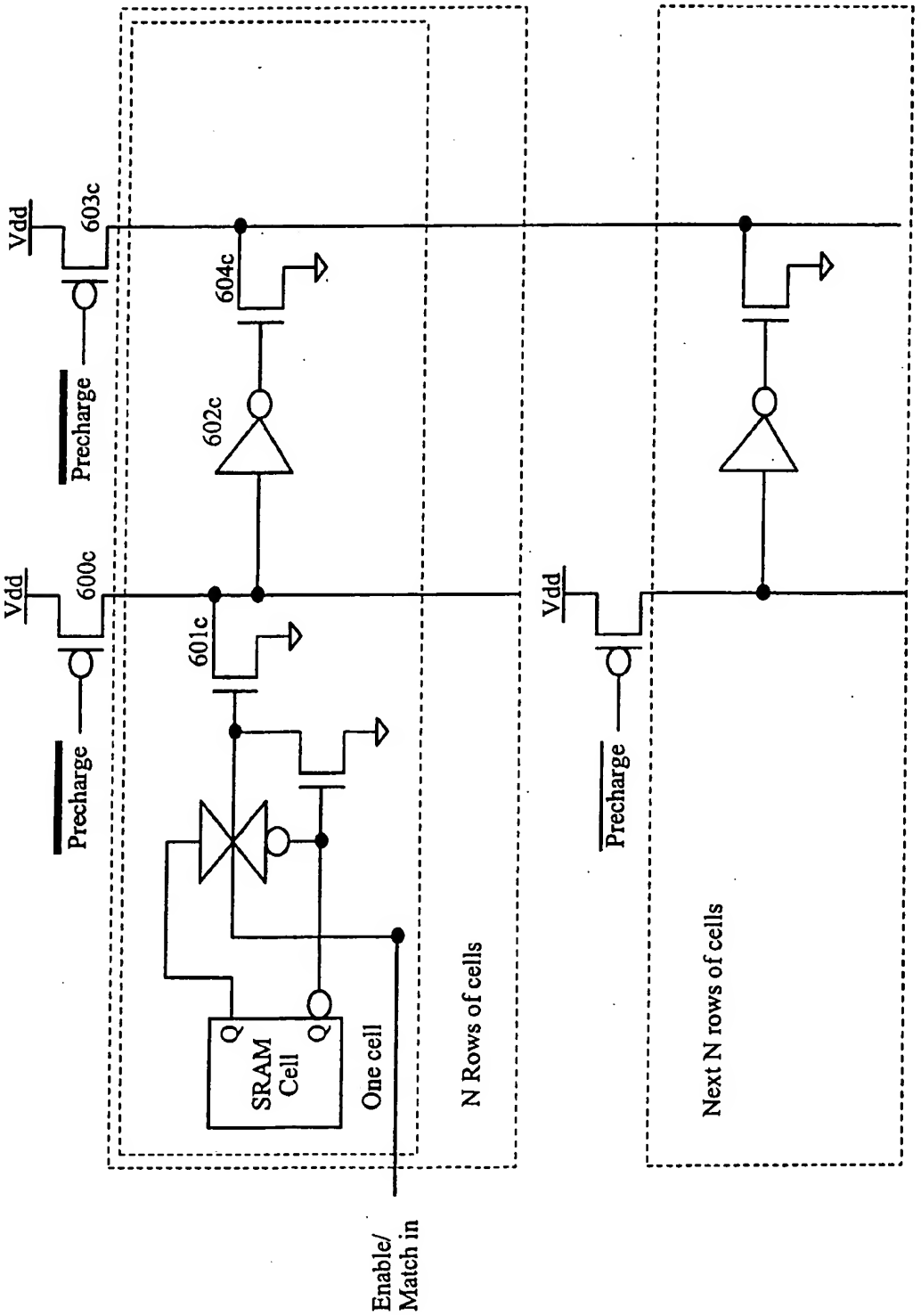
Vdd
603c
604c
602c
Precharge
Vdd
600c
601c
Precharge
Q
SRAM Cell
Q
One cell
N Rows of cells
Enable/ Match in
Vdd
Precharge
Next N rows of cells

FIGURE 6C

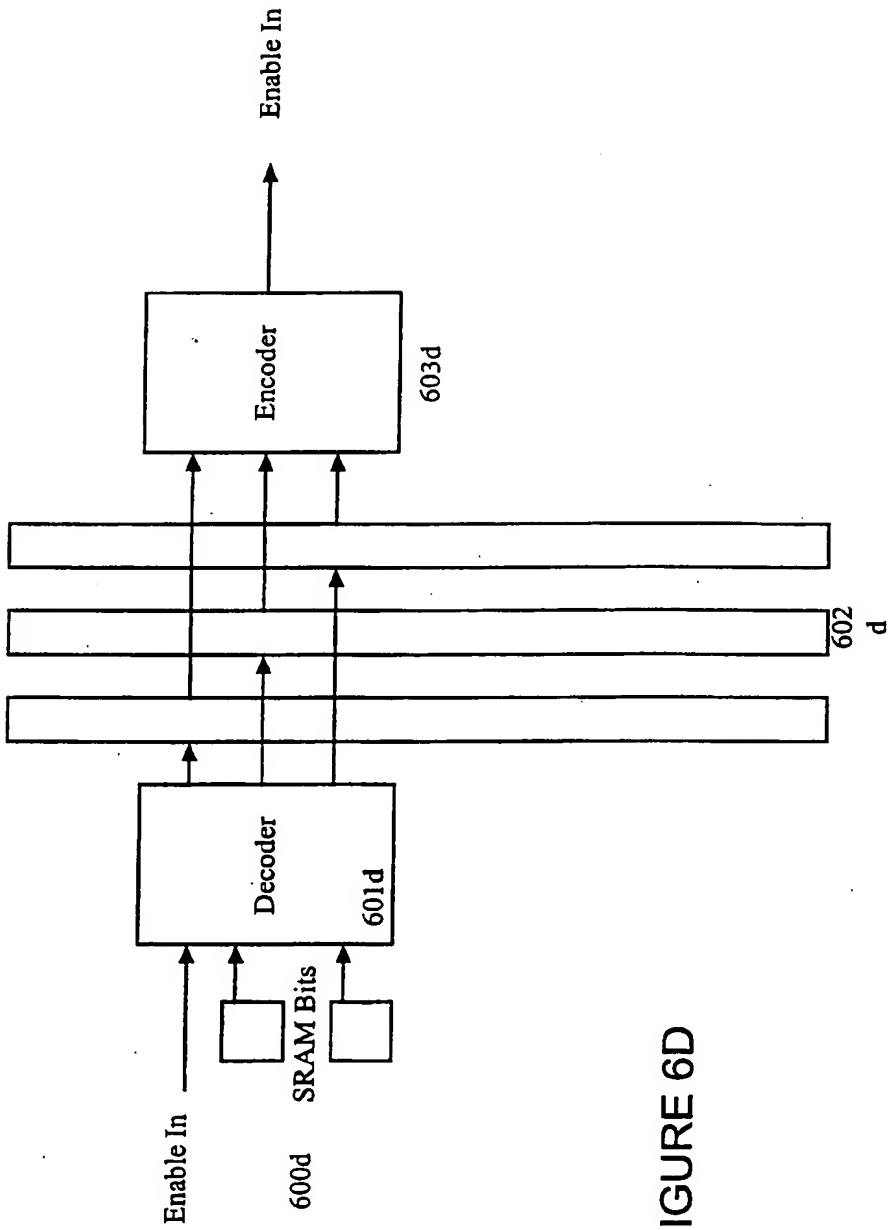
Enable In
Encoder
603d
602
d
Decoder
601d
Enable In
SRAM Bits
600d

FIGURE 6D

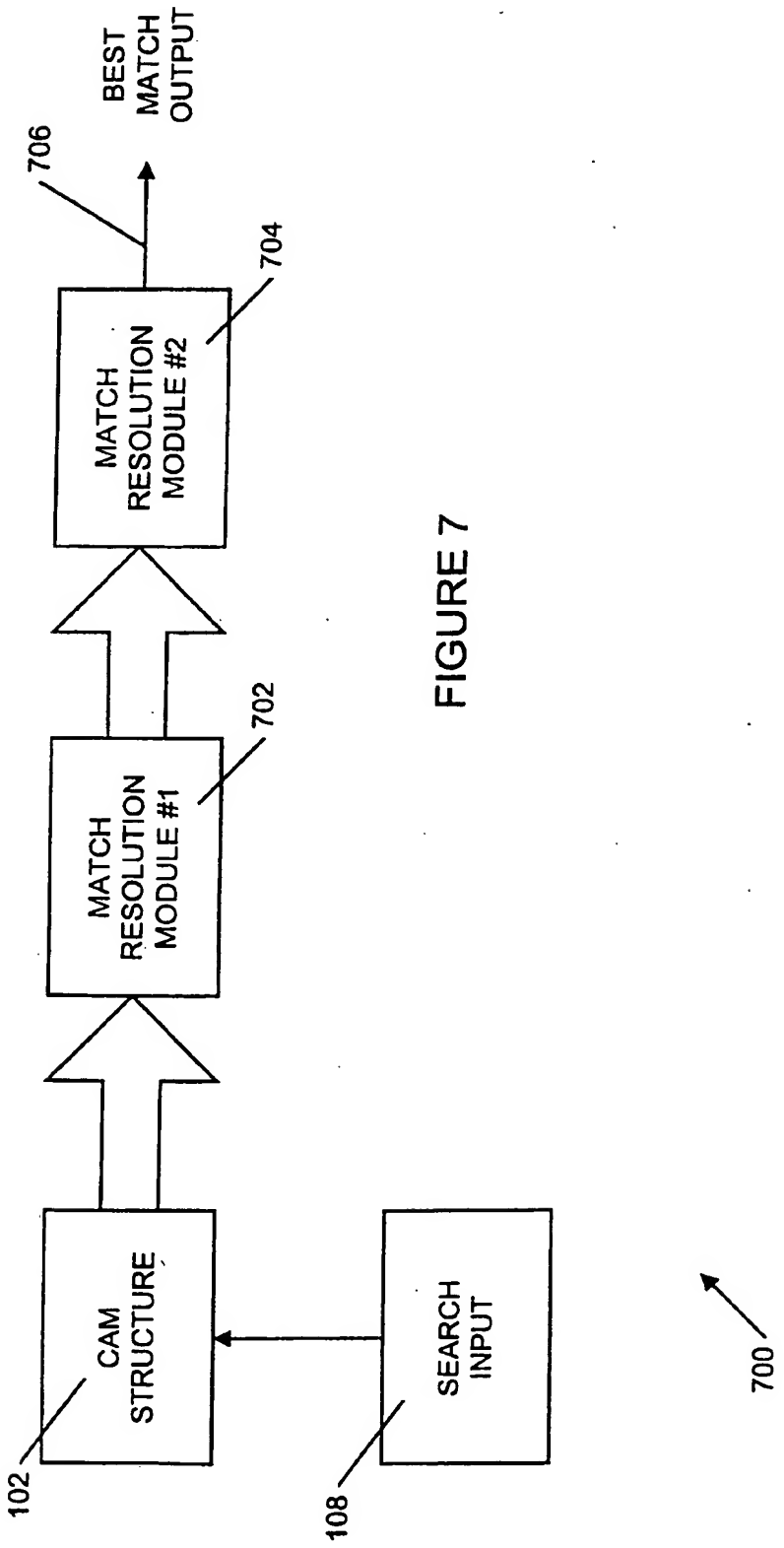
BEST MATCH OUTPUT
706
704
MATCH RESOLUTION MODULE #2
702
MATCH RESOLUTION MODULE #1
CAM STRUCTURE
102
SEARCH INPUT
108
700

FIGURE 7

# INTERNATIONAL SEARCH REPORT

Int. ional Application No
PCT/US 00/22002

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C15/00 G11C15/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
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| X | JP 11 102589 A (NIPPON TELEGR &TELEPH CORP <NTT>) 13 April 1999 (1999-04-13)<br>the whole document | 1,2,7, 10-12, 16-21, 23-25, 27,29 |
| X | EP 0 622 805 A (PLESSEY SEMICONDUCTORS LTD) 2 November 1994 (1994-11-02)<br>abstract<br>figures 4,5<br>column 1, line 1 -column 2, line 8 | 1,9 |
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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 9 November 2000 | 22/11/2000 |

| Name and mailing address of the ISA | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,<br>Fax: (+31-70) 340-3016 | Colling, P |

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Inte nal Application No
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| A | US 5 555 397 A (SASAMA HIROSHI ET AL) 10 September 1996 (1996-09-10) column 4, line 40 -column 6, line 40 figure 1 | 8 |

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Information on patent family members

Int[illegible]nal Application No
PCT/US 00/22002

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
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